1. Description

This Power MOSFET is produced using KIA's advanced planar stripe DMOS technology.

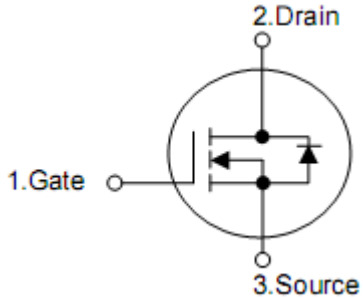
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters and high efficiency switching for power management in portable and battery operated products.

2. Features

- 35A, 60V, $R_{DS(on)Typ}$=15mΩ @ V_{GS}=10V
- Low gate charge (typical 33nC)
- High ruggedness
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

3. Pin configuration

TO-252



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KND8606B	TO-252	KIA

5. Absolute maximum ratings

TC=25℃ unless otherwise specified

Parameter		Symbol	Ratings	Units
Drain-Source Voltage		V_{DSS}	60	V
Drain Current	T_C=25°C	I_D	35	A
	T_C=100°C		22	A
Drain Current —Pulsed [1]		I_{DM}	80	A
Gate-Source Voltage		V_{GSS}	±20	V
Single Pulsed Avalanche Energy [2]		EAS	450	mJ
Avalanche Current [1]		I_{AR}	35	A
Repetitive Avalanche Energy [1]		E_{AR}	12	mJ
Peak Diode Recovery dv/dt [3]		dv/dt	4.5	V/ns
Power Dissipation	T_C=25°C	P_D	60	W
	Derate above 25°C		0.8	W/°C
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C
Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		T_L	300	°C

6. Thermal characteristics

Parameter	Symbol	Ratings	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Case-to-Sink Typ.	$R_{\theta JS}$	-	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

7. Electrical characteristics

(TJ=25°C,unless otherwise notes)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	60	-	-	V
Breakdown Voltage Temperature Coefficient	ΔBV_{DSS} / ΔT_J	I_D=250uA, Referenced to 25°C	-	0.06	-	V/℃
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V	-	-	1	uA
		V_{DS}=48V,T_C=150°C	-	-	10	uA
Gate-Body Leakage Current, Forward	I_{GSSF}	V_{GS}=20V,V_{DS}=0V	-	-	100	nA
Gate-Body Leakage Current, Reverse	I_{GSSR}	V_{GS}=-20V,V_{DS}=0V	-	-	-100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250uA	1	1.8	2.5	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=20A	-	15	20	mΩ
Forward Transconductance	g_{FS}	V_{DS}=25V,I_D=25A [4]	-	22	-	S
Input Capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1.0MHz	-	2800	-	pF
Output Capacitance	C_{oss}		-	200	-	pF
Reverse Transfer Capacitance	C_{rss}		-	100	-	pF
Turn-On Delay Time	$t_{d(on)}$	V_{DD}=30V,I_D=25A, R_G=25Ω [4),5)]	-	15	-	ns
Turn-On Rise Time	t_r		-	105	-	ns
Turn-Off Delay Time	$t_{d(off)}$		-	60	-	ns
Turn-Off Fall Time	t_f		-	65	-	ns
Total Gate Charge	Q_g	V_{DS}=48V,I_D=25A, V_{GS}=10V [4),5)]	-	33	-	nC
Gate-Source Charge	Q_{gs}		-	8.5	-	nC
Gate-Drain Charge	Q_{gd}		-	14	-	nC
Maximum Continuous Drain-Source Diode Forward Current	I_S	-	-	-	35	A
Maximum Pulsed Drain-Source Diode Forward Current	I_{SM}	-	-	-	80	A
Drain-Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=35A	-	-	1.4	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V,I_S=35A, dI_F/dt=100A/us [4)]	-	60	-	ns
Reverse Recovery Charge	Q_{rr}		-	80	-	nC

Notes：
1) Repetitive Rating : Pulse width limited by maximum junction temperature
2) I_{AS}=35A, V_{DD}=50V, R_G=25Ω, Starting T_J=25°C
3) I_{SD}≤35A, di/dt≤200A/us, V_{DD}≤BV_{DSS}, Starting T_J=25°C
4) Pulse Test：Pulse width≤300us, Duty cycle≤2%
5) Essentially independent of operating temperature

8. Typical Characteristics

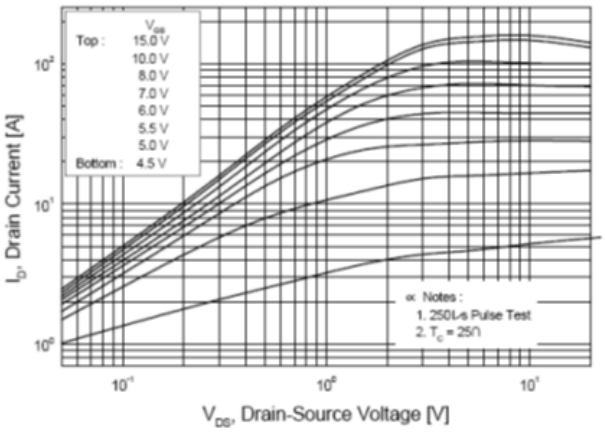


Figure 1. On-Region Characteristics

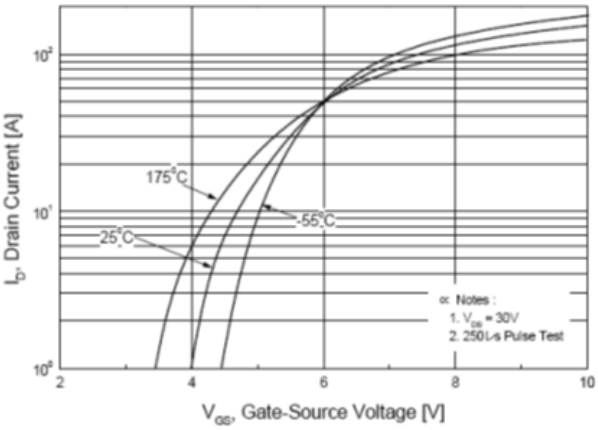


Figure 2. Transfer Characteristics

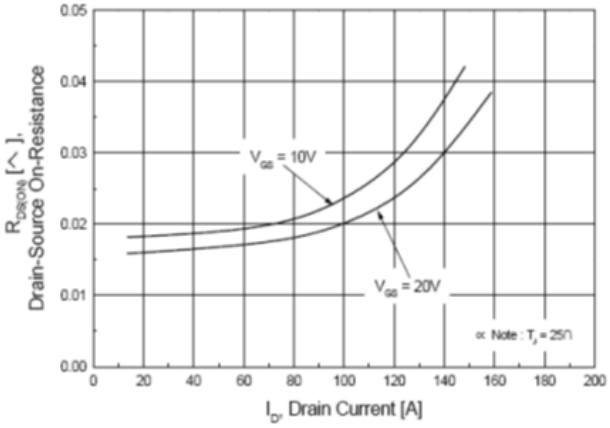


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

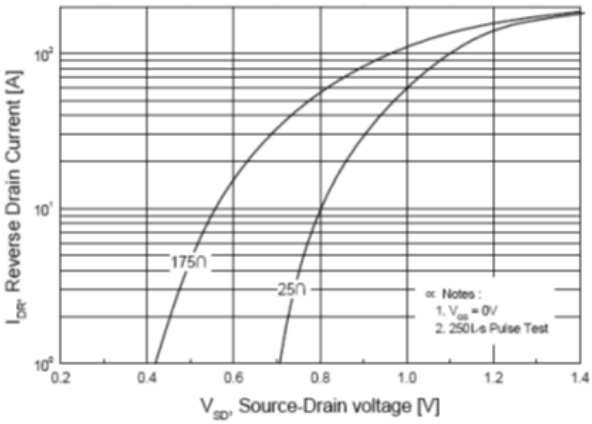


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

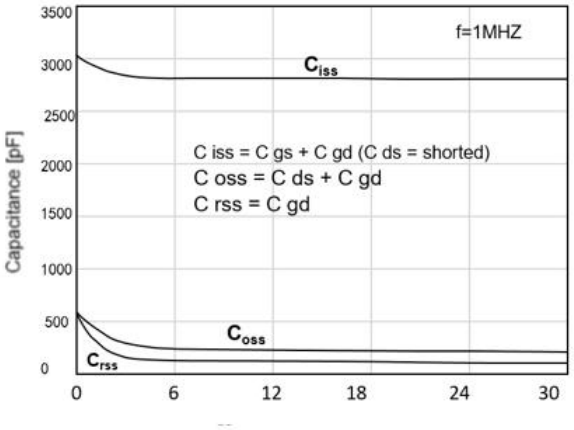


Figure 5. Capacitance Characteristics

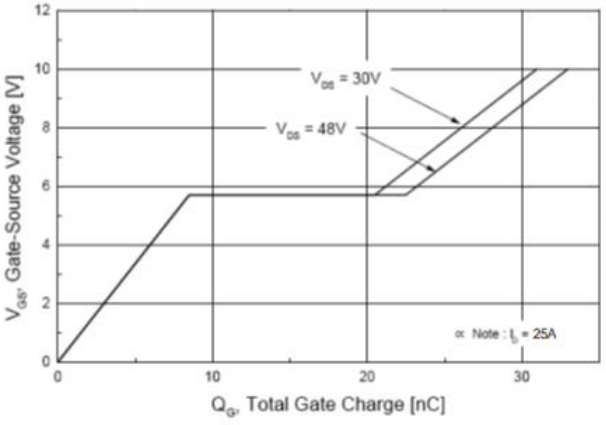


Figure 6. Gate Charge Characteristics

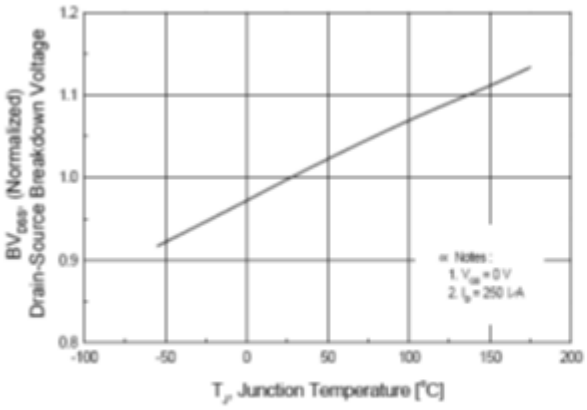


Figure 7. Breakdown Voltage Variation vs Temperature

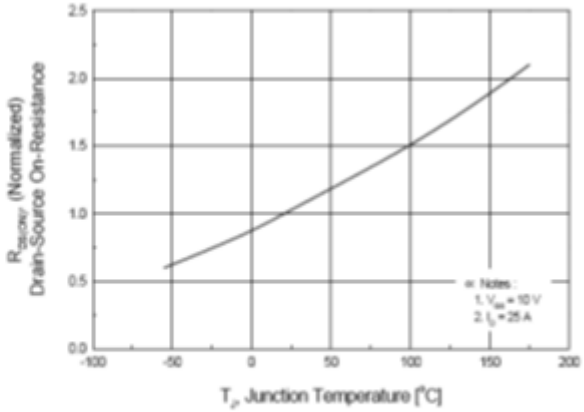


Figure 8. On-Resistance Variation vs Temperature

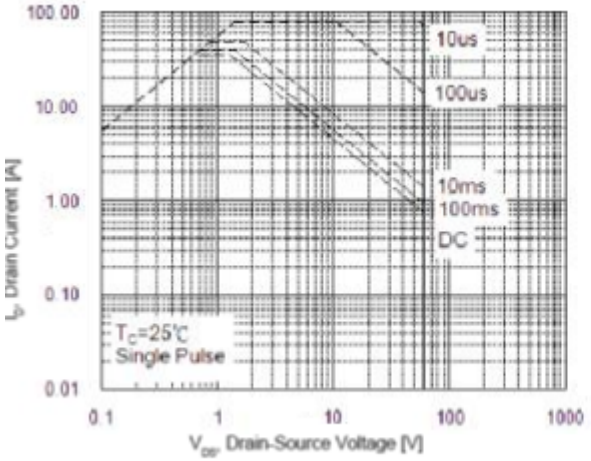


Figure 9. Maximum Safe Operating Area

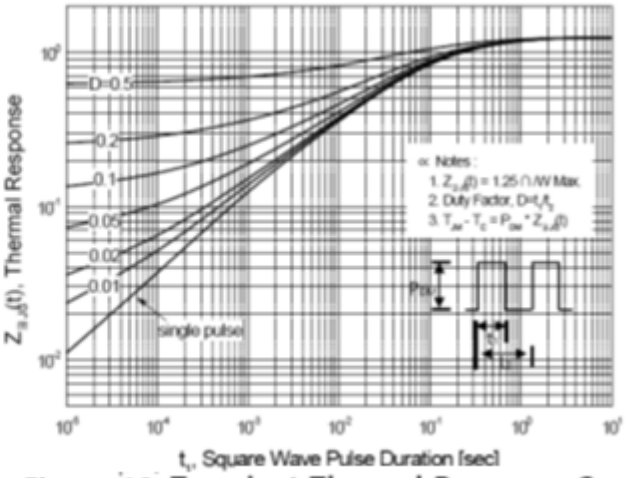
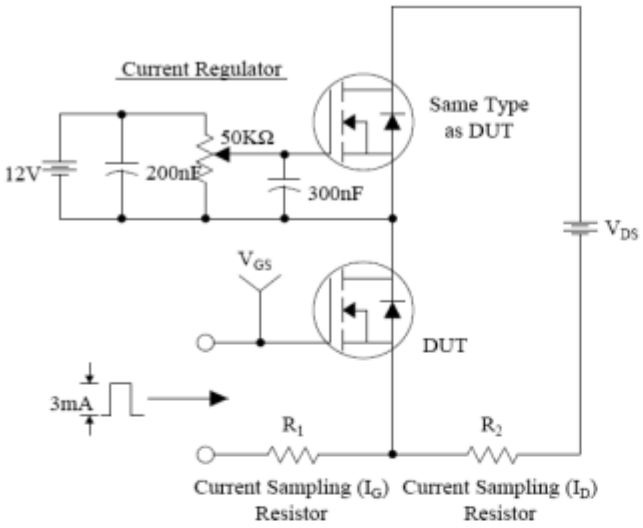
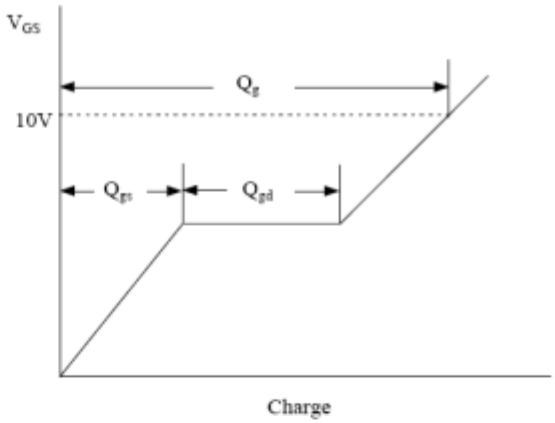


Figure 10. Transient Thermal Response Curve

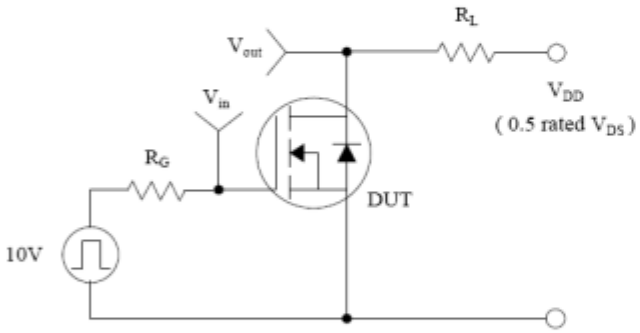
9. Test Circuits and Waveforms

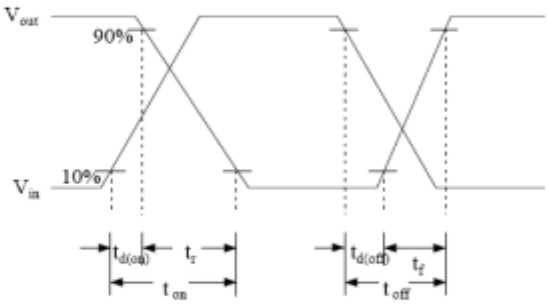
Gate Charge Test Circuit & Waveform



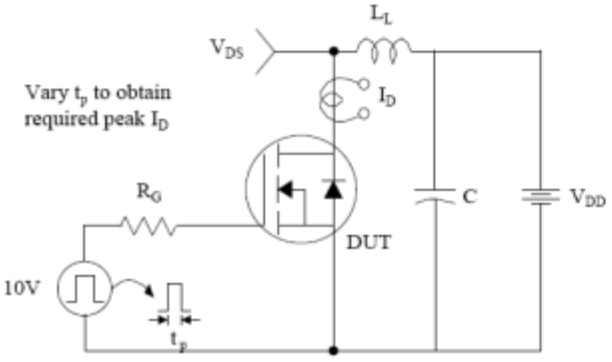


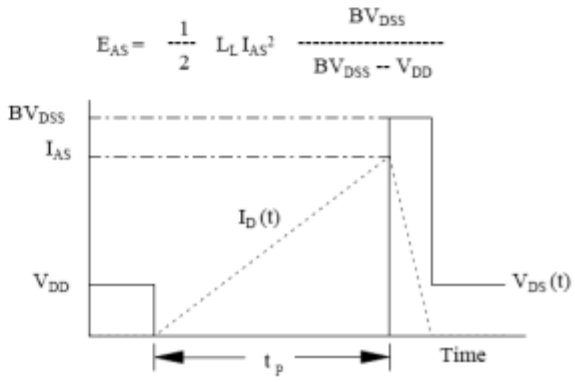
Resistive Switching Test Circuit & Waveforms





Unclamped Inductive Switching Test Circuit & Waveforms





Peak Diode Recovery dv/dt Test Circuit & Waveforms