

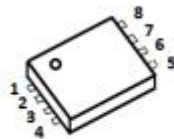
## 1. Features

- n  $R_{DS(ON),typ.}=7.0m\Omega@V_{GS}=10V$
- n Super low gate charge
- n Excellent Cdv/dt effect decline
- n Advanced high cell density trench technology

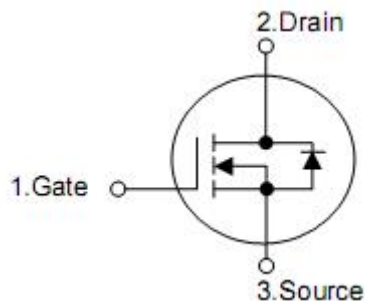
## 2. Applications

- n Motor control and drive
- n Battery management
- n UPS (Uninterruptible Power Supplies)

## 3. Pin configuration



DFN5\*6



Pin	Function
4	Gate
5,6,7,8	Drain
1,2,3	Source

## 4. Ordering Information

Part Number	Package	Brand
KNY3406C	DFN5*6	KIA

## 5. Absolute maximum ratings

Parameter	Symbol	Ratings	Unit
Drain-to-Source Voltage	$V_{DSS}$	60	V
Continuous Drain Current $V_{GS}@10V^1$	$T_C=25\text{ }^\circ\text{C}$	80	A
	$T_C=100\text{ }^\circ\text{C}$	47	
Pulsed Drain Current <sup>2</sup>	$I_{DM}$	280	
Avalanche Energy single pulse <sup>3</sup>	$E_{AS}$	80	mJ
Gate-Source voltage	$V_{GS}$	$\pm 20$	V
Power dissipation (TC = 25°C)	$P_D$	41	W
Junction & Storage Temperature Range	$T_J, T_{STG}$	-55 to 150	°C

## 6. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance, junction-ambient <sup>1</sup>	$R_{\theta JA}$	62	°C/W
Thermal resistance, Junction-case <sup>1</sup>	$R_{\theta JC}$	1.4	

## 7. Electrical characteristics

(T<sub>J</sub>=25°C, unless otherwise notes)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	
Static characteristics							
Drain-source breakdown voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	60	-	-	V	
Gate threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.3	1.9	2.5	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V	T <sub>J</sub> =25°C	-	-	1	μA
			T <sub>J</sub> =125°C	-	-	10	
Gate leakage current	I <sub>GSS</sub>	V <sub>GS</sub> =20V, V <sub>DS</sub> =0V	-	-	100	nA	
Drain-source on-resistance <sup>2</sup>	R <sub>DSON</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =10A T <sub>J</sub> =25°C	-	7.0	8.5	mΩ	
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =5A T <sub>J</sub> =25°C	-	9.5	12	mΩ	
Dynamic characteristics							
Gate Resistance	R <sub>G</sub>	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz	-	1.2	-	Ω	
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> =30V, V <sub>GS</sub> =0V, F=1MHz	-	3300	-	pF	
Output capacitance	C <sub>oss</sub>		-	200	-	pF	
Reverse transfer capacitance	C <sub>rss</sub>		-	150	-	pF	
Turn-on delay time	t <sub>d(on)</sub>		-	16	-	ns	
Rise time	t <sub>r</sub>	V <sub>GS</sub> =10V, V <sub>DD</sub> =30V, R <sub>G</sub> =3.3Ω, I <sub>D</sub> =20A,	-	41	-	ns	
Turn-off delay time	t <sub>d(off)</sub>		-	56	-	ns	
Fall time	t <sub>f</sub>		-	16	-	ns	
Gate Charge Characteristics							
Total gate charge	Q <sub>g</sub>	V <sub>GS</sub> =10V, V <sub>DS</sub> =30V, I <sub>D</sub> =18A, F=1MHz	-	55	-	nC	
Gate-source charge	Q <sub>gs</sub>		-	8.5	-	nC	
Gate-drain charge	Q <sub>gd</sub>		-	14	-	nC	
Diode characteristics							
Continuous Source Current <sup>1,5</sup>	I <sub>S</sub>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	-	-	80	A	
Diode forward voltage <sup>2</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>SD</sub> =5A	-	-	1.3	V	
Reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> =20A dI/dt=100A/μs	-	20	-	ns	
Reverse recovery charge	Q <sub>rr</sub>		-	70	-	nC	

Note:1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

2. The data tested by pulsed, pulse width ≤300us, duty cycle ≤2%.

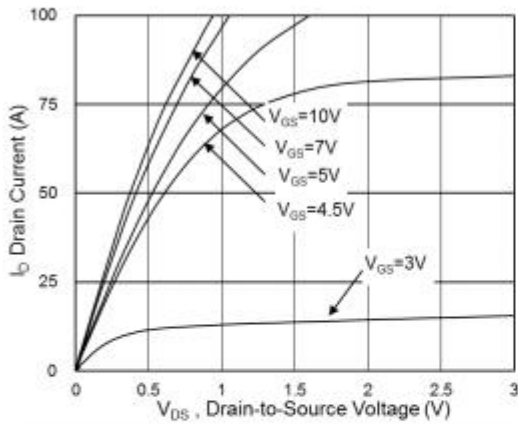
3. The EAS data shows Max.rating. The test condition is V<sub>DD</sub>=50V, V<sub>GS</sub>=10V, L=0.1mH, I<sub>AS</sub>=40A.

4. The power dissipation is limited by 150 °C junction temperature.

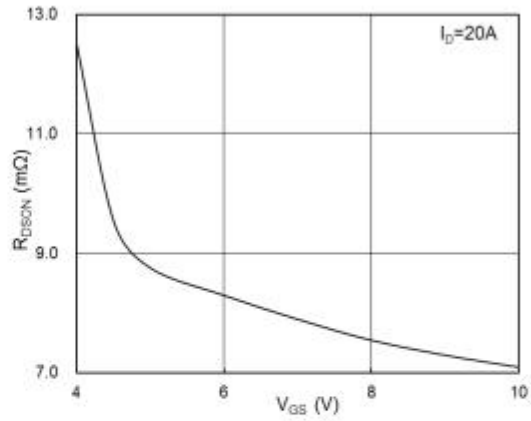
5. The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub>, in real applications, should be limited by total power dissipation

**8. Typical Characteristics**

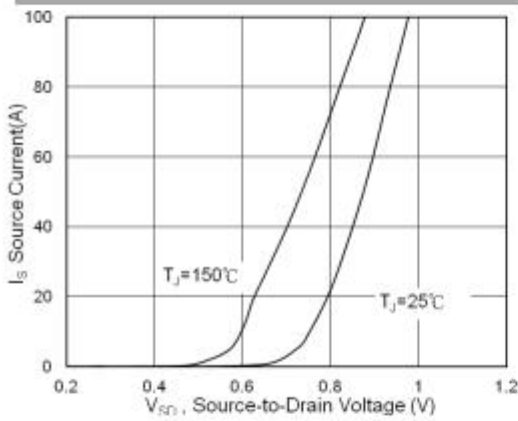
**Typical Characteristics**



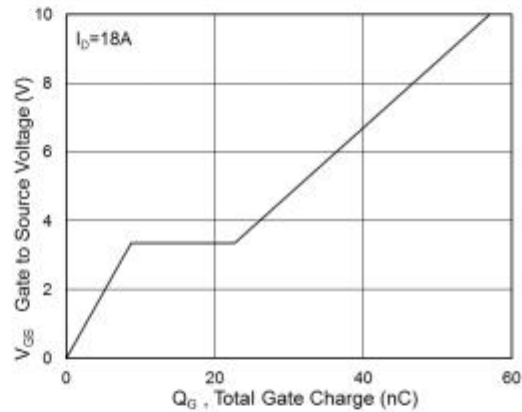
**Fig.1 Typical Output Characteristics**



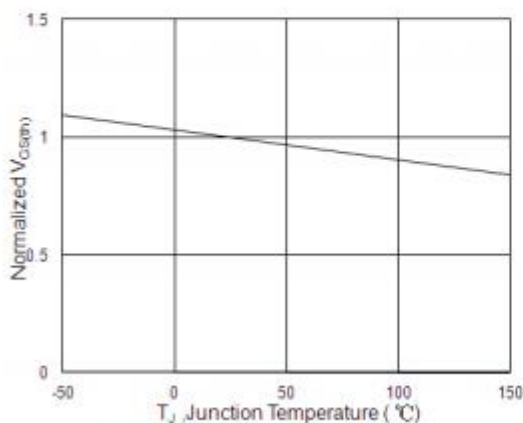
**Fig.2 On-Resistance vs Gate-Source Voltage**



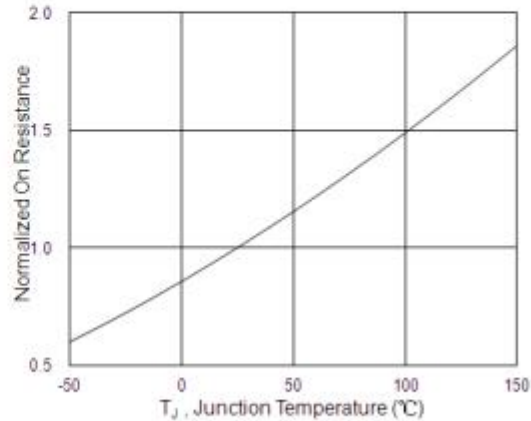
**Fig.3 Forward Characteristics of Reverse**



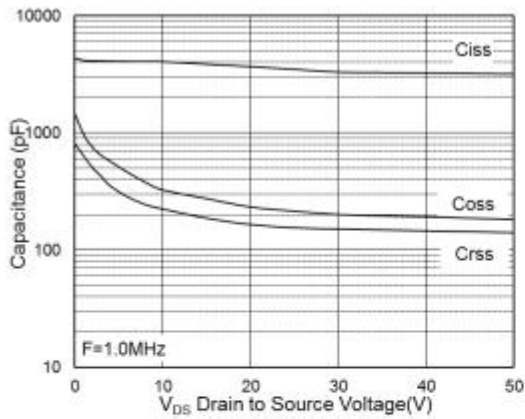
**Fig.4 Gate-Charge Characteristics**



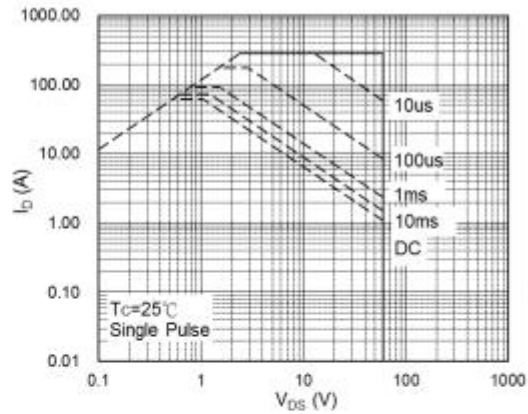
**Fig.5 Normalized  $V_{GS(th)}$  vs  $T_J$**



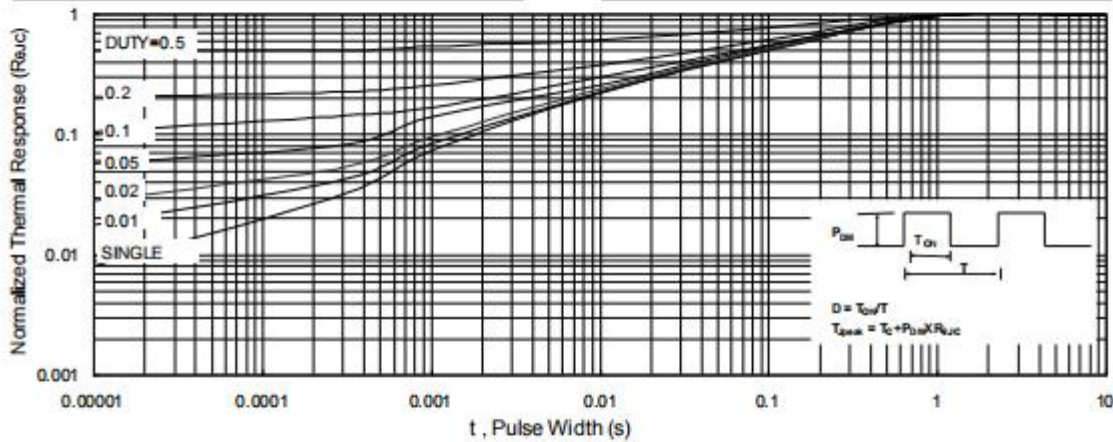
**Fig.6 Normalized  $R_{DS(on)}$  vs  $T_J$**



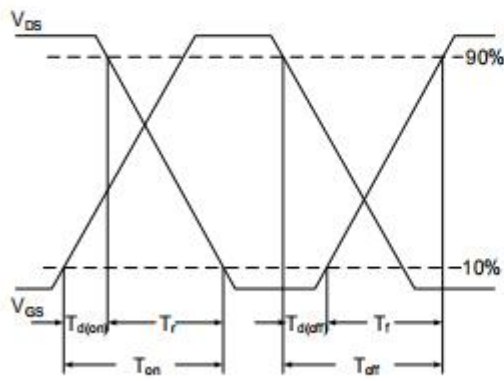
**Fig.7 Capacitance**



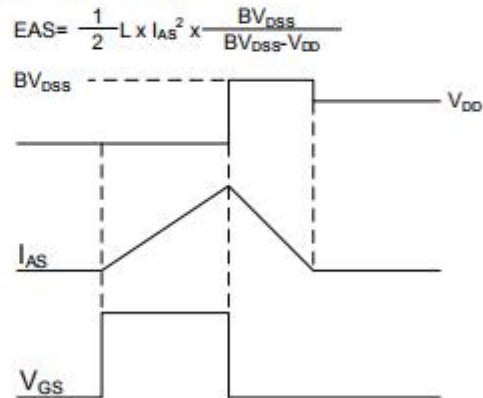
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**