## 1. Features

- SGT MOSFET technology
- Proprietary New Trench Technology
- $R_{DS(ON)}$=2.0mΩ(typ.)@$V_{GS}$=10V, DFN5*6
- $R_{DS(ON)}$=3.1mΩ(typ.)@$V_{GS}$=10V, TO-252
- Fast Switching and High efficiency
- Low on-resistance

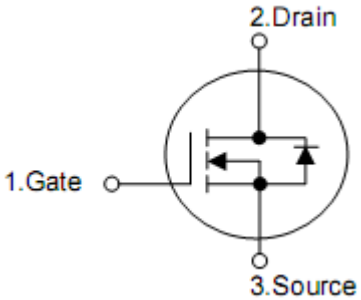
## 2. Applications

- Synchronous Rectification for AC/DC Quick Charger
- Battery management
- Telecom and Server Power Supply

## 3. Pin configuration


DFN5*6


TO-252




| Pin | | Function |
|---|---|---|
| DFN5*6 | TO-252 | |
| 4 | 1 | Gate |
| 5,6,7,8 | 2 | Drain |
| 1,2,3 | 3 | Source |

## 4. Ordering Information

| Part Number | Package | Brand |
|---|---|---|
| KCY2408A | DFN5*6 | KIA |
| KCD2408A | TO-252 | KIA |

## 5. Absolute maximum ratings

($T_C$=25 ºC, unless otherwise specified)

| Parameter | | Symbol | Ratings | Unit |
|---|---|---|---|---|
| Drain-to-Source Voltage [1] | | $V_{DSS}$ | 80 | V |
| Gate-to-Source Voltage | | $V_{GSS}$ | ±20 | V |
| Continuous Drain Current | Tc=25 ºC | $I_D$ | 190 | A |
| | Tc=100 ºC | $I_D$ | 143 | A |
| Pulsed Drain Current at $V_{GS}$=10V [2] | | $I_{DM}$ | 750 | A |
| Single Pulse Avalanche Energy L=1mH | | EAS | 880 | mJ |
| Power Dissipation $T_C$=25 ºC | | $P_D$ | 227 | W |
| Derating Factor above $T_A$=25°C | | $P_D$ | 1.82 | W/°C |
| Maximum Temperature for Soldering<br>Leads at 0.063in (1.6mm) from Case for 10 seconds,<br>Package Body for 10 seconds | | $T_L$<br>$T_{PAK}$ | 300<br>260 | ºC |
| Operating and Storage Temperature Range | | $T_J$&$T_{STG}$ | -55 to 150 | ºC |

Caution: Stresses greater than those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device.

## 6. Thermal characteristics

| Parameter | Symbol | Ratings | Unit |
|---|---|---|---|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 0.55 | ºC/W |
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 50 | ºC/W |

## 7. Electrical characteristics

($T_J$=25°C,unless otherwise specified)

| Parameter | Symbol | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| Drain-to-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=250uA | | 80 | - | - | V |
| Drain-to-Source Leakage Current | $I_{DSS}$ | $V_{DS}$=80V, $V_{GS}$=0V | | - | - | 1 | uA |
| | | $V_{DS}$=64V,$T_J$=125°C | | - | - | 100 | uA |
| Gate-to-Source Leakage Current | $I_{GSS}$ | $V_{GS}$=±20V, $V_{DS}$=0V | | - | - | ±100 | nA |
| Drain-to-Source ON Resistance [3] | $R_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=40A | DFN5*6 | - | 2.0 | 2.5 | mΩ |
| | | | TO-252 | - | 3.1 | 3.5 | mΩ |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{DS}$=$V_{GS}$,$I_D$=250uA | | 2.0 | - | 4.0 | V |
| Forward Transconductance [4] | gfs | $V_{DS}$=15V,$I_D$=25A | | - | 18 | - | S |
| Input Capacitance | $C_{iss}$ | $V_{GS}$=0V,$V_{DS}$=40V, f=1.0MHZ | | - | 6670 | - | pF |
| Reverse Transfer Capacitance | $C_{rss}$ | | | - | 54 | - | |
| Output Capacitance | $C_{oss}$ | | | - | 1020 | - | |
| Total Gate Charge | $Q_g$ | $V_{DD}$=40V,$I_D$=50A, $V_{GS}$=10V | | - | 105 | - | nC |
| Gate-to-Source Charge | $Q_{gs}$ | | | - | 28 | - | |
| Gate-to-Drain (Miller) Charge | $Q_{gd}$ | | | - | 29 | - | |
| Turn-on Delay Time | $t_{d(ON)}$ | $V_{DD}$=40V, $I_D$=50A, $R_G$=3.0Ω,$V_{GS}$=10V | | - | 30 | - | nS |
| Rise Time | $t_{rise}$ | | | - | 20 | - | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 65 | - | |
| Fall Time | $t_{fall}$ | | | - | 18 | - | |
| Continuous Source Current [4] | $I_{SD}$ | Integral PN-diode in MOSFET | | - | - | 190 | A |
| Pulsed Source Current [4] | $I_{SM}$ | | | - | - | 750 | A |
| Forward Voltage | $V_{SD}$ | $I_S$=80A, $V_{GS}$=0V | | - | - | 1.2 | V |
| Reverse recovery time | $t_{rr}$ | $V_{GS}$=0V ,$I_F$=50A, diF/dt=100A/μs | | - | 82 | - | ns |
| Reverse recovery charge | $Q_{rr}$ | | | - | 71 | - | uC |

Note:
1) $T_J$=+25°C to +150°C
2) Repetitive rating; pulse width limited by maximum junction temperature.
3) Pulse width≤380μs; duty cycle≤2%.
4) Silicon limited current only.

## 8. Test circuits and waveforms

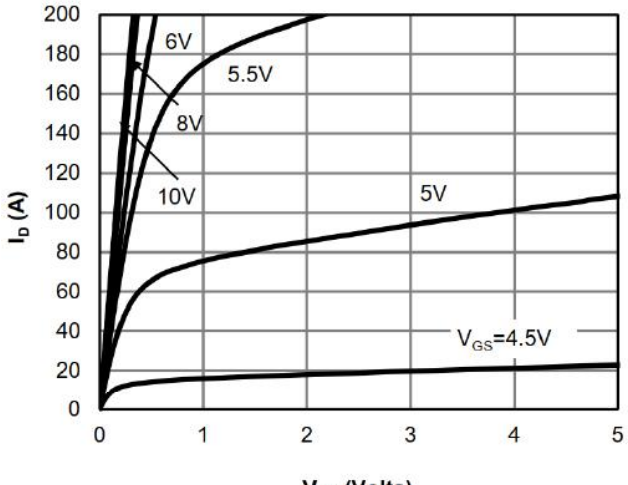



Figure 1: On-Region Characteristics

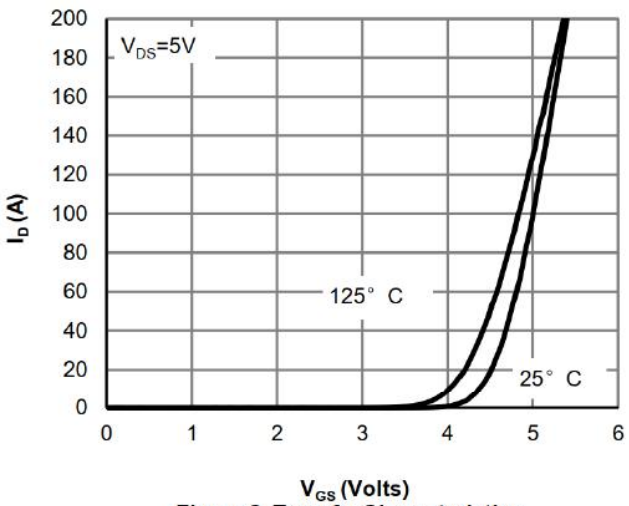



Figure 2: Transfer Characteristics

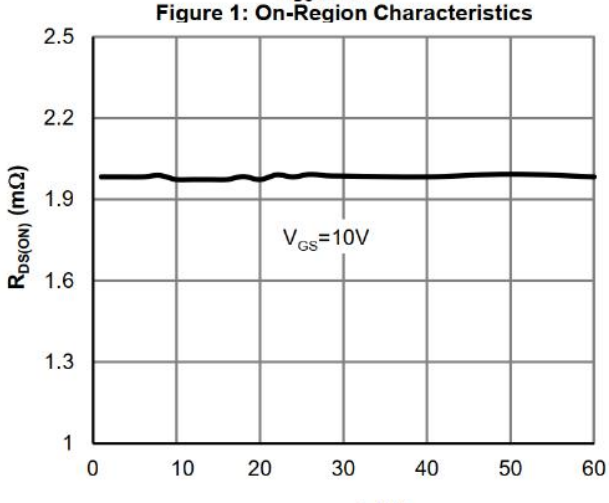



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

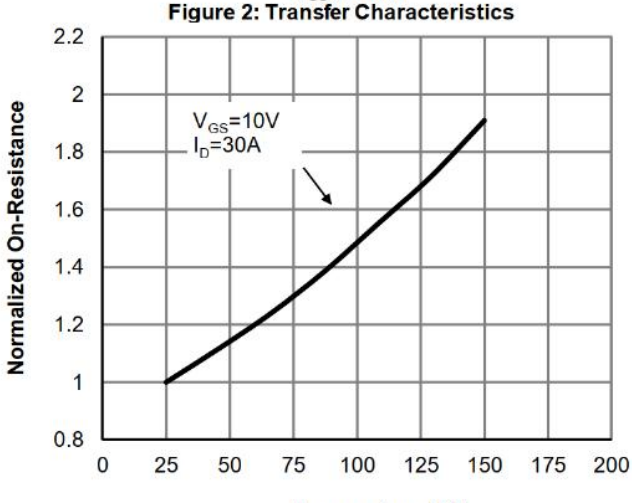



Figure 4: On-Resistance vs. Junction Temperature

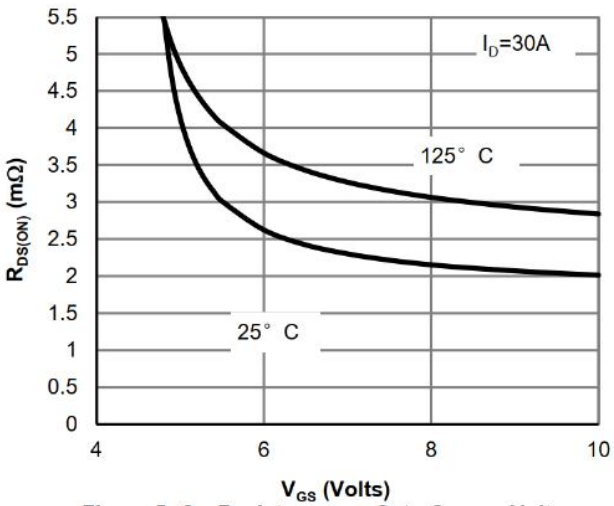



Figure 5: On-Resistance vs. Gate-Source Voltage

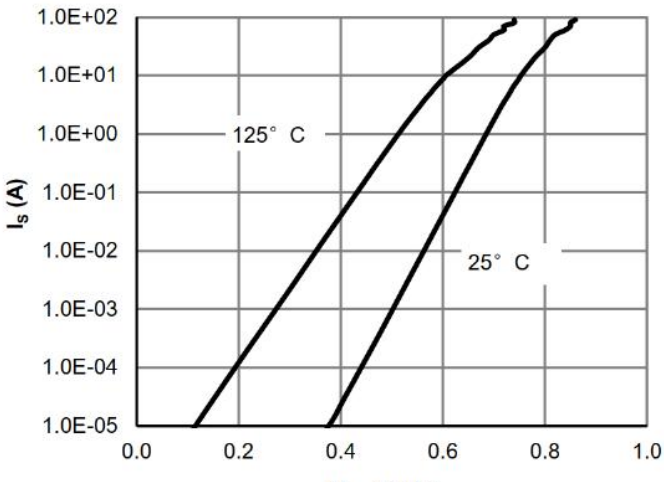



Figure 6: Body-Diode Characteristics

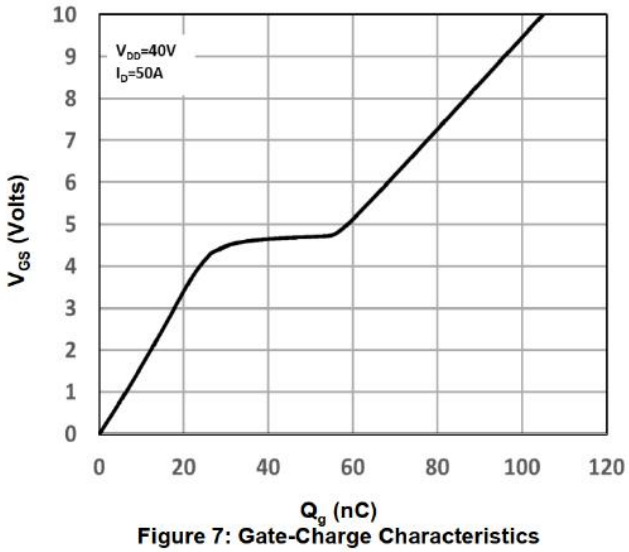



Figure 7: Gate-Charge Characteristics

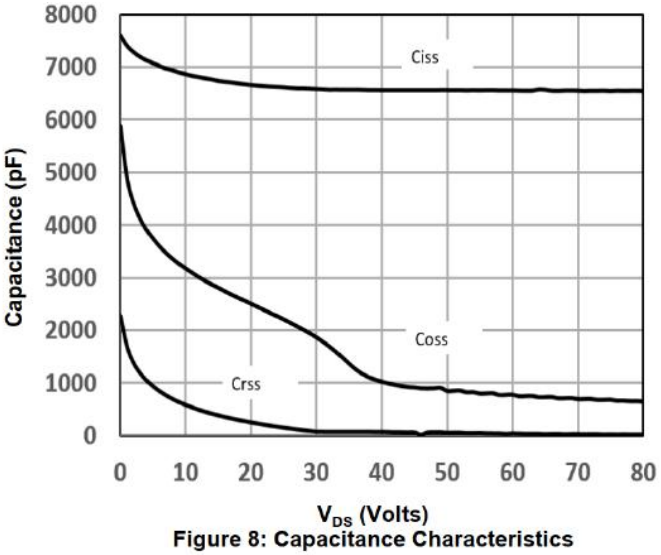



Figure 8: Capacitance Characteristics

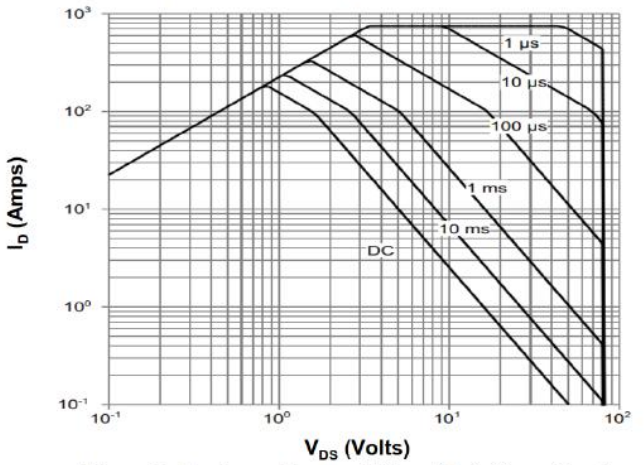



Figure 9: Maximum Forward Biased Safe Operating Area

## 9. Test Circuits and Waveforms

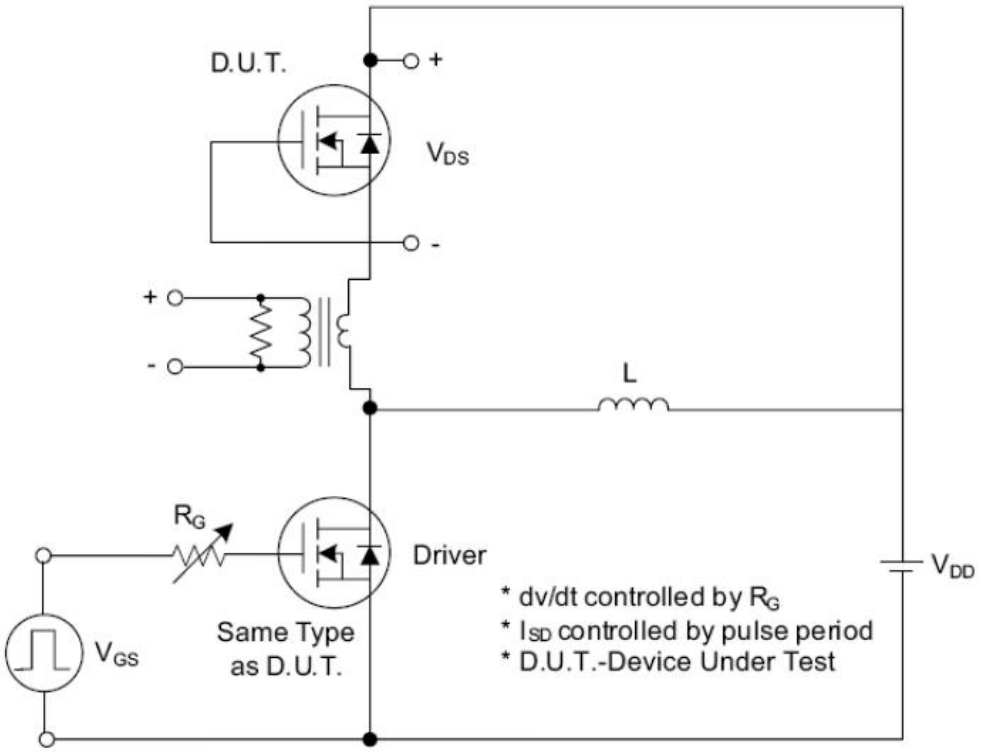



Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

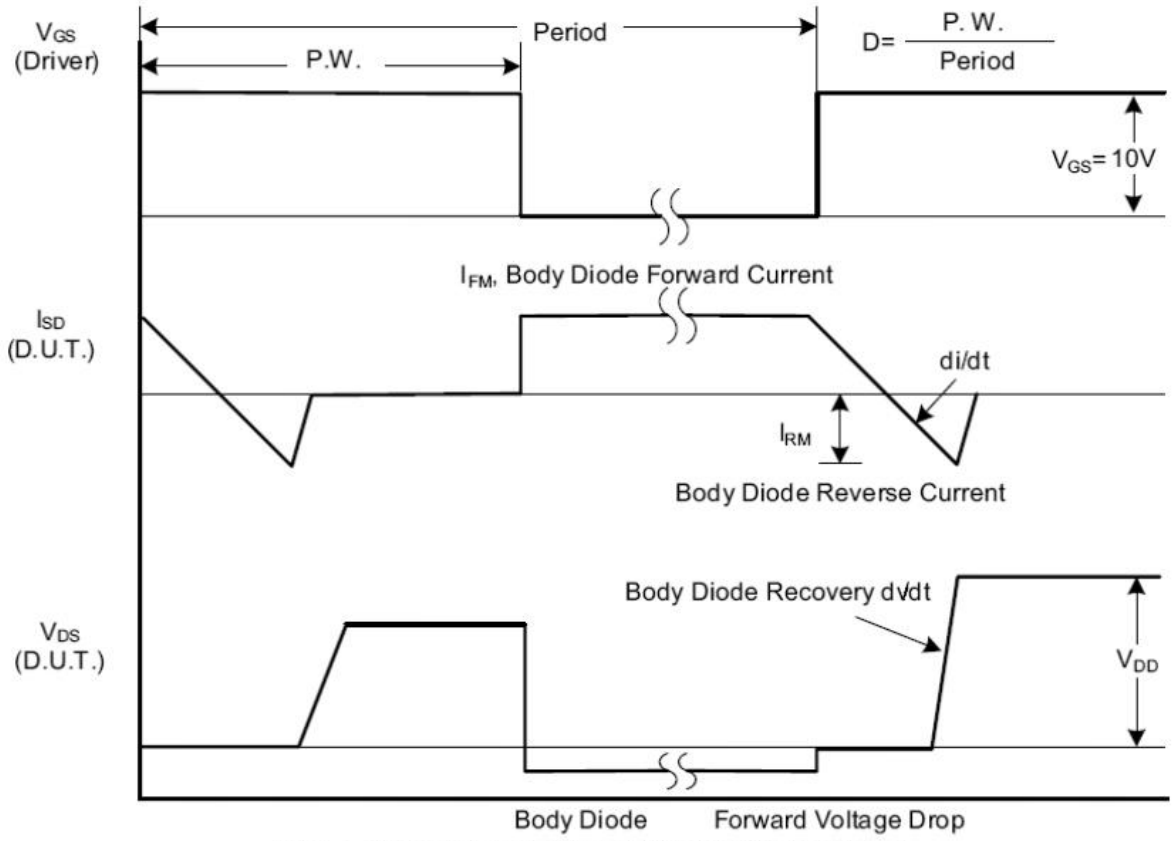



Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

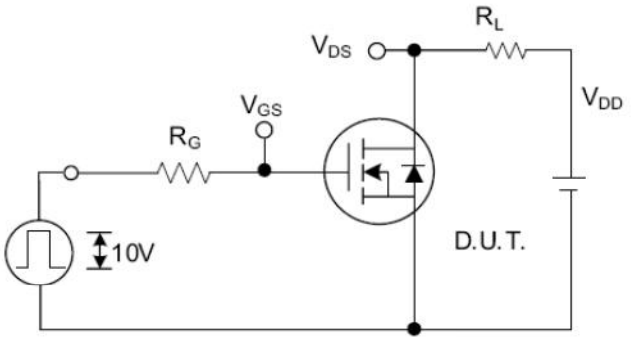



Fig. 2.1 Switching Test Circuit

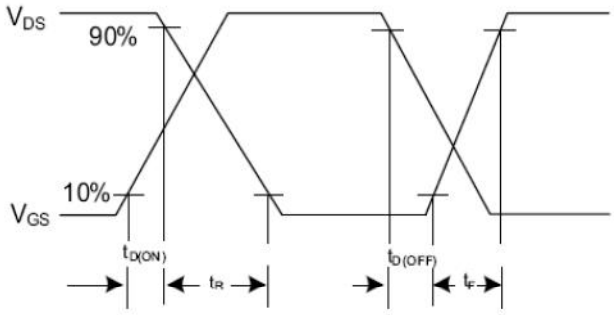



Fig. 2.2 Switching Waveforms

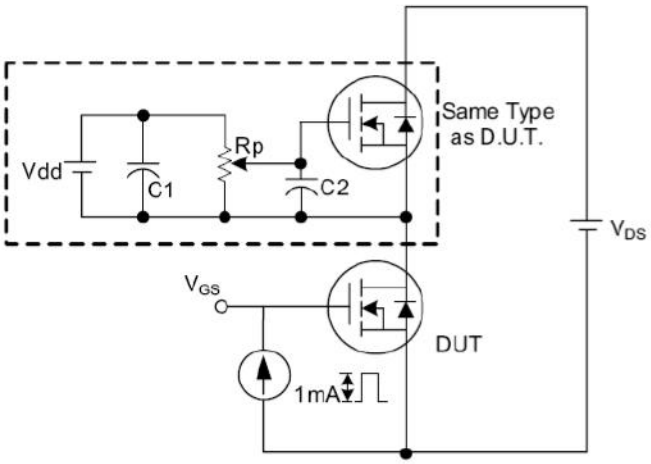



Fig. 3 . 1 Gate Charge Test Circuit

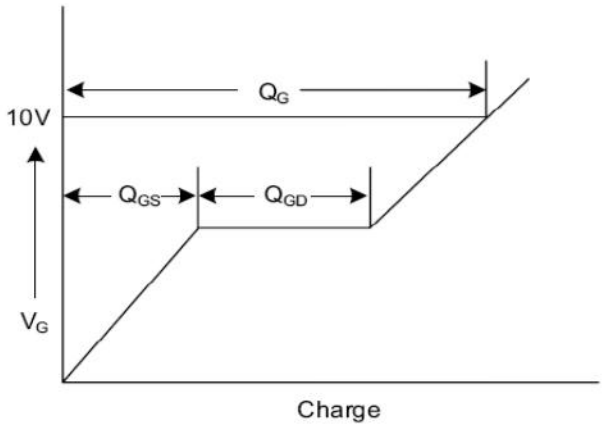



Fig. 3 . 2 Gate Charge Waveform

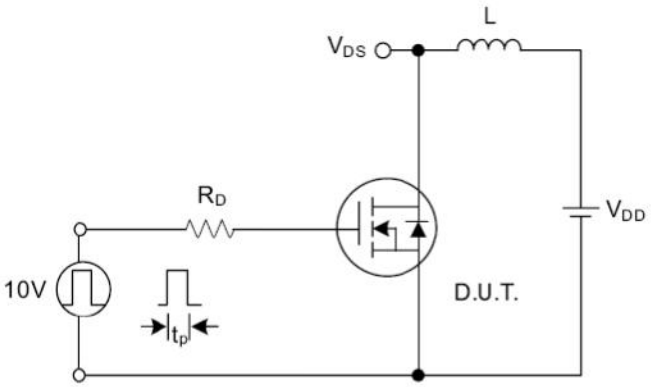



Fig. 4.1 Unclamped Inductive Switching Test Circuit

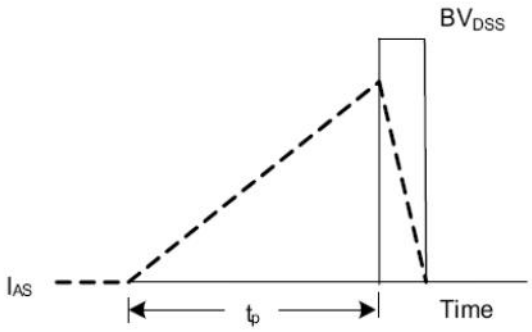



Fig. 4.2 Unclamped Inductive Switching Waveforms