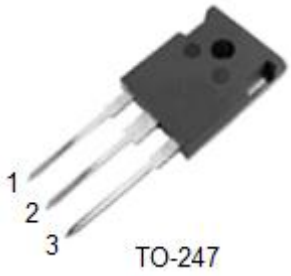
1. Features

- Advanced Planar Process
- $R_{DS(ON)}$=0.75Ω(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Rugged Polysilicon Gate Structure

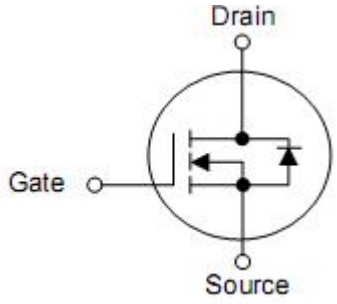
2. Applications

- BLDC Motor Driver
- Electric Welder
- High Efficiency SMPS

3. Symbol



TO-247



Pin	Function
1	Gate
2	Drain
3	Source

4. Ordering Information

Part Number	Package	Brand
KNM6390A	TO-247	KIA

5. Absolute maximum ratings

T_C=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain-source voltage		V_{DSS}	900	V
Gate-to-Source Voltage		V_{GSS}	±30	V
Continuous drain current	T_C=25°C	I_D	12	A
	T_C=100°C	I_D	7.5	A
Pulsed Drain Current at V_{GS}=10V [2,4]		I_{DM}	48	A
Single pulse avalanche energy		E_{AS}	1200	mJ
Peak Diode Recovery dv/dt [3]		dv/dt	5.0	V/ns
Power dissipation		P_D	175	W
Derate above 25°C			1.4	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T_L T_{PAK}	300 260	°C
Operating junction and storage temperature range		T_J ,T_{STG}	-55 to150	ºC

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance junction-case	$R_{\theta JC}$	0.714	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	55	ºC/W

7. Electrical characteristics

(T_J=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	900	-	-	V
Drain-source leakage current	I_{DSS}	V_{DS}=900V, V_{GS}=0V	-	-	1	uA
		V_{DS}=720V, T_C=125°C			125	
Gate-source forward leakage	I_{GSS}	V_{GS}=±30V, V_{DS}=0V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=6A	-	0.75	1.0	Ω
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.0	-	4.0	V
Forward Transconductance	gfs	V_{DS}=25V,I_D=6A	-	32	-	S
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz	-	3002	-	pF
Reverse transfer capacitance	C_{rss}		-	75	-	pF
Output capacitance	C_{oss}		-	248	-	pF
Total gate charge	Q_g	V_{DD}=450V, I_D=12A V_{GS}=0~10V	-	84	-	nC
Gate-source charge	Q_{gs}		-	17	-	nC
Gate-drain charge	Q_{gd}		-	33	-	nC
Turn-on delay time	$t_{d(on)}$	V_{DD}=450V,V_{GS}=10V, R_G=10Ω, I_D=12A		26		ns
Rise time	t_r			80		ns
Turn-off delay time	$t_{d(off)}$			66		ns
Fall time	t_f			78		ns
Continuous Source Current [2)]	I_{SD}	Integral PN-diode in MOSFET			12	A
Pulsed Source Current[2)]	I_{SM}		-	-	48	
Diode forward voltage	V_{SD}	I_S=12A,V_{GS}=0V,	-	-	1.5	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V,I_F=12A, dI_F/dt=100A/μs [4)]	-	550	-	nS
Reverse Recovery Charge	Q_{rr}		-	4.5	-	nC

Note:
1) T_J=+25 ºC to +150 ºC
2) Silicon limited current only.
3) Package limited current.
4) Repetitive rating; pulse width limited by maximum junction temperature.
5) Pulse width≤380us; duty cycle≤2%.

8. Typical operating characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

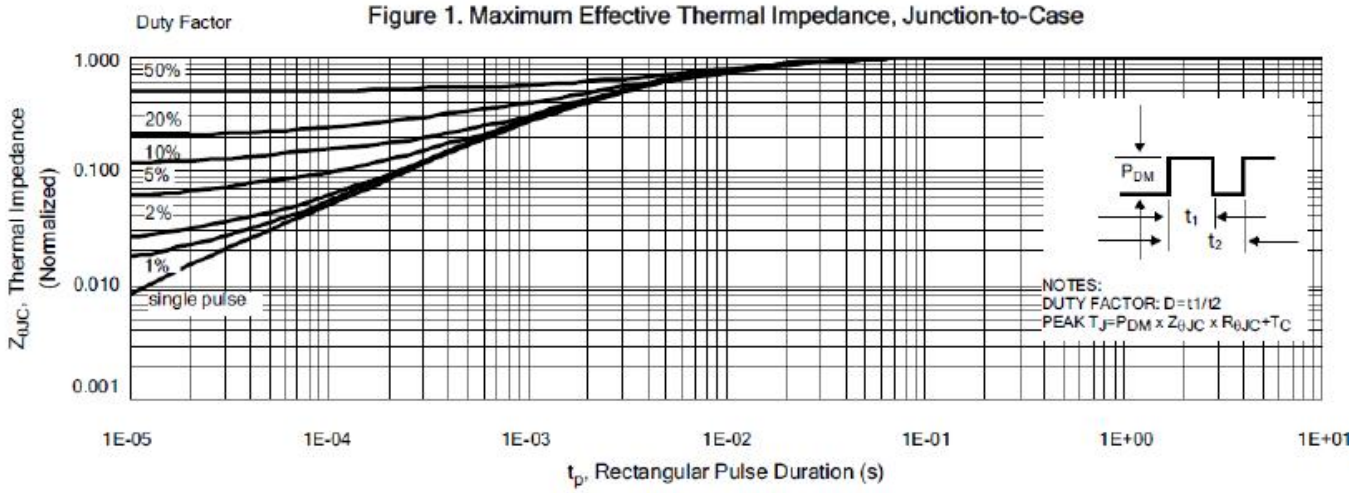


Figure 2. Maximum Power Dissipation vs Case Temperature

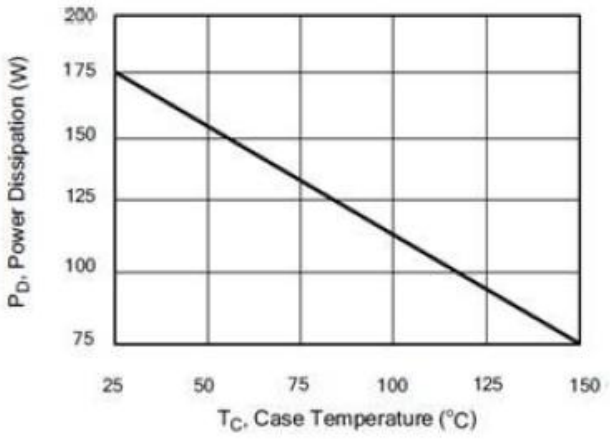


Figure3. Maximum Continuous Drain Current vs Case Temperature

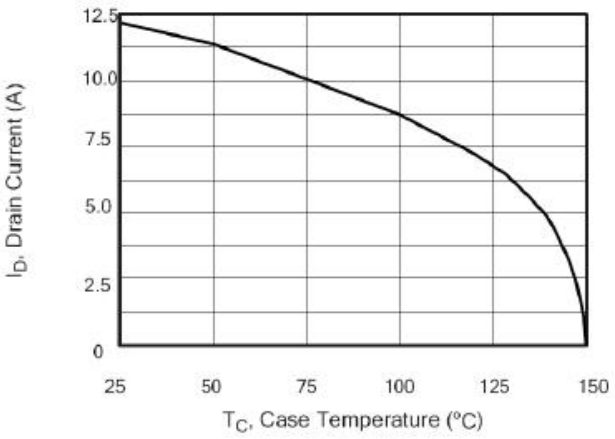


Figure 4. Typical Output Characteristics

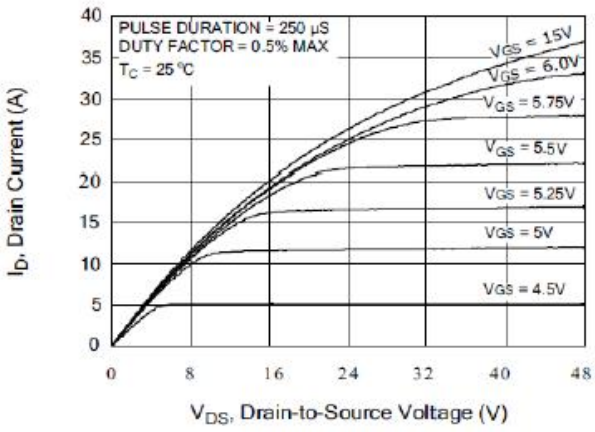


Figure5. Typical Drain-to-Source ON Resistance vs Gate Voltage and Drain Current

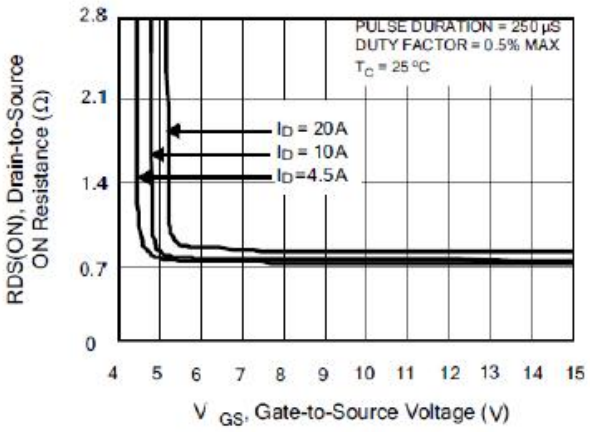


Figure 6. Maximum Peak Current Capability

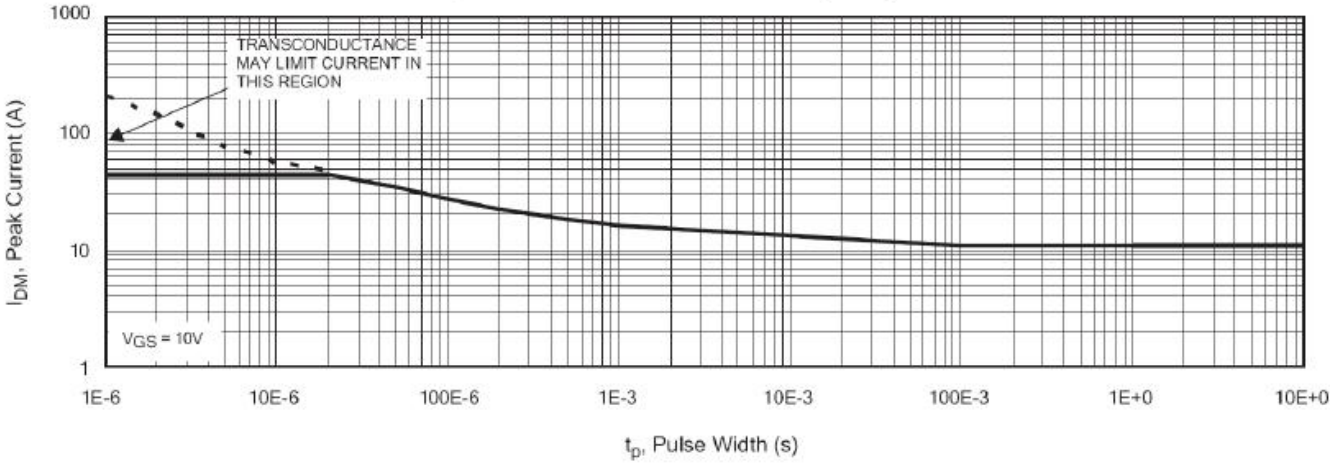


Figure 7. Typical Transfer Characteristics

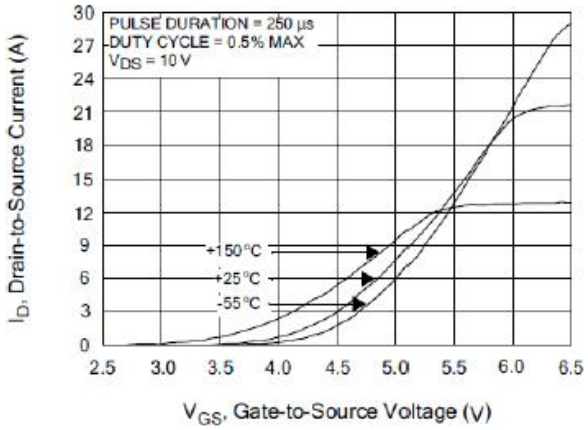


Figure8. Unclamped Inductive Switching Capability

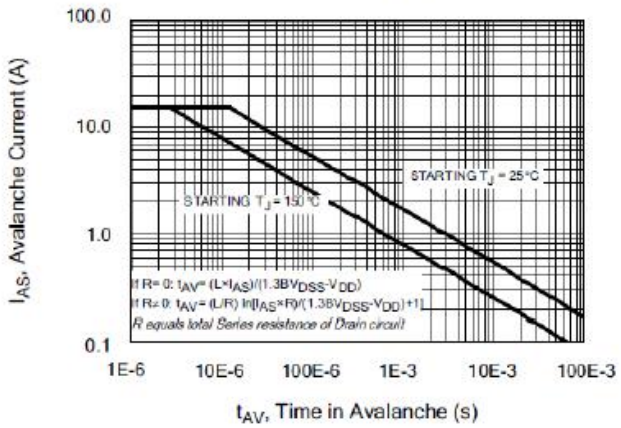


Figure 9. Typical Drain-to-Source ON Resistance vs Drain Current

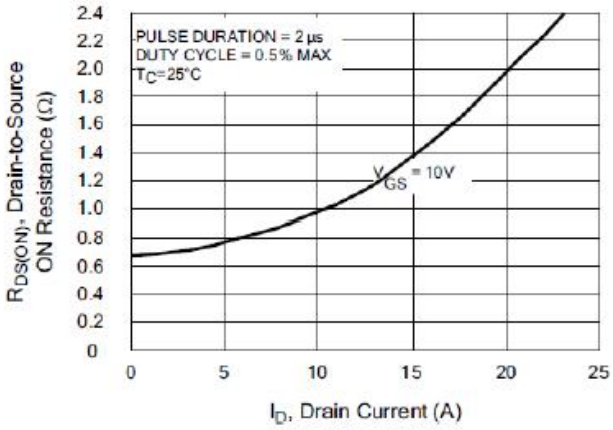


Figure 10. Typical Drain-to-Source ON Resistance vs Junction Temperature

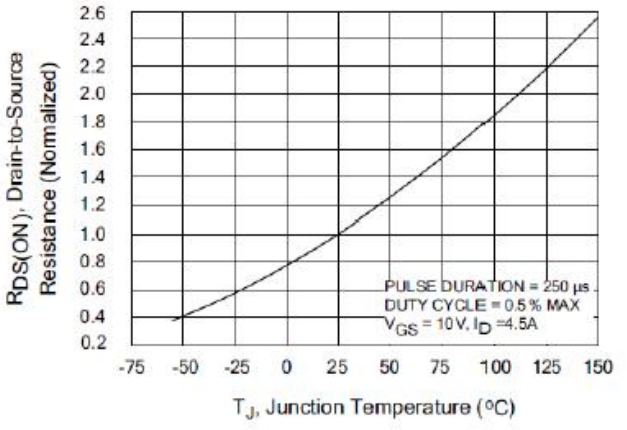


Figure 11. Typical Breakdown Voltage vs Junction Temperature

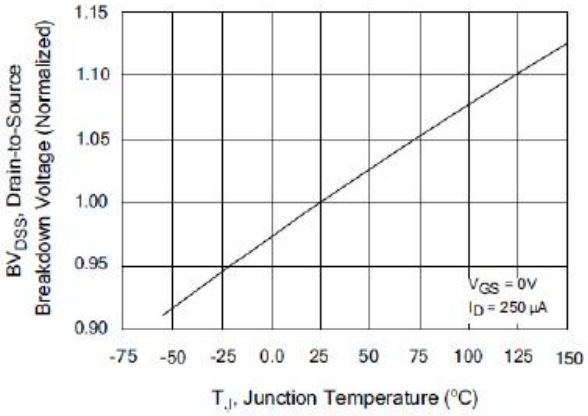


Figure 12. Typical Threshold Voltage vs Junction Temperature

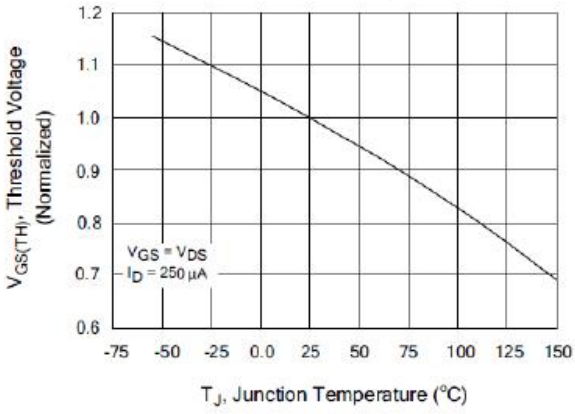


Figure 13. Maximum Forward Bias Safe Operating Area

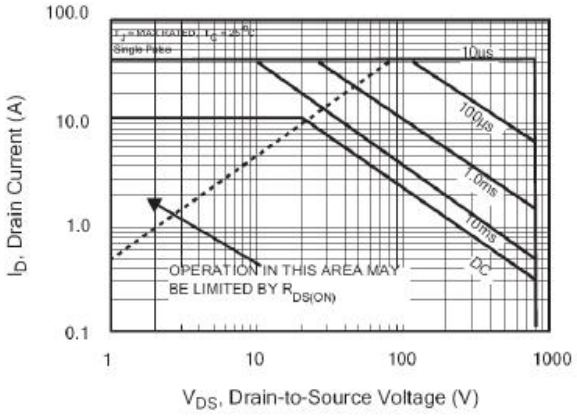
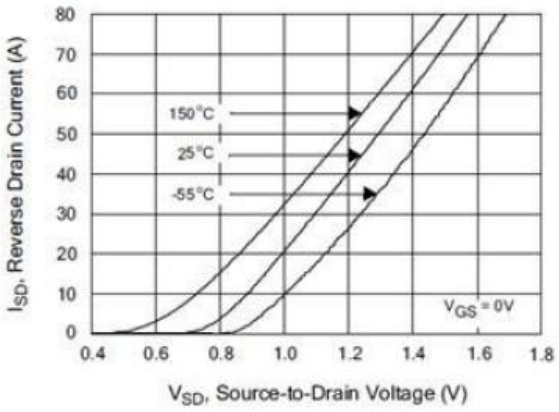


Figure 14 Typical Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

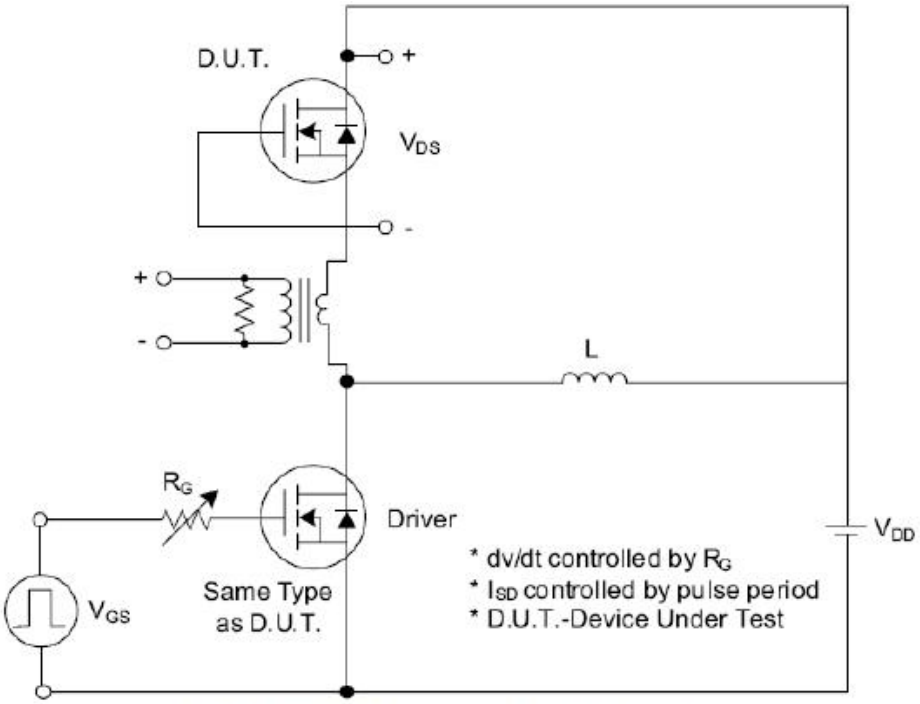


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

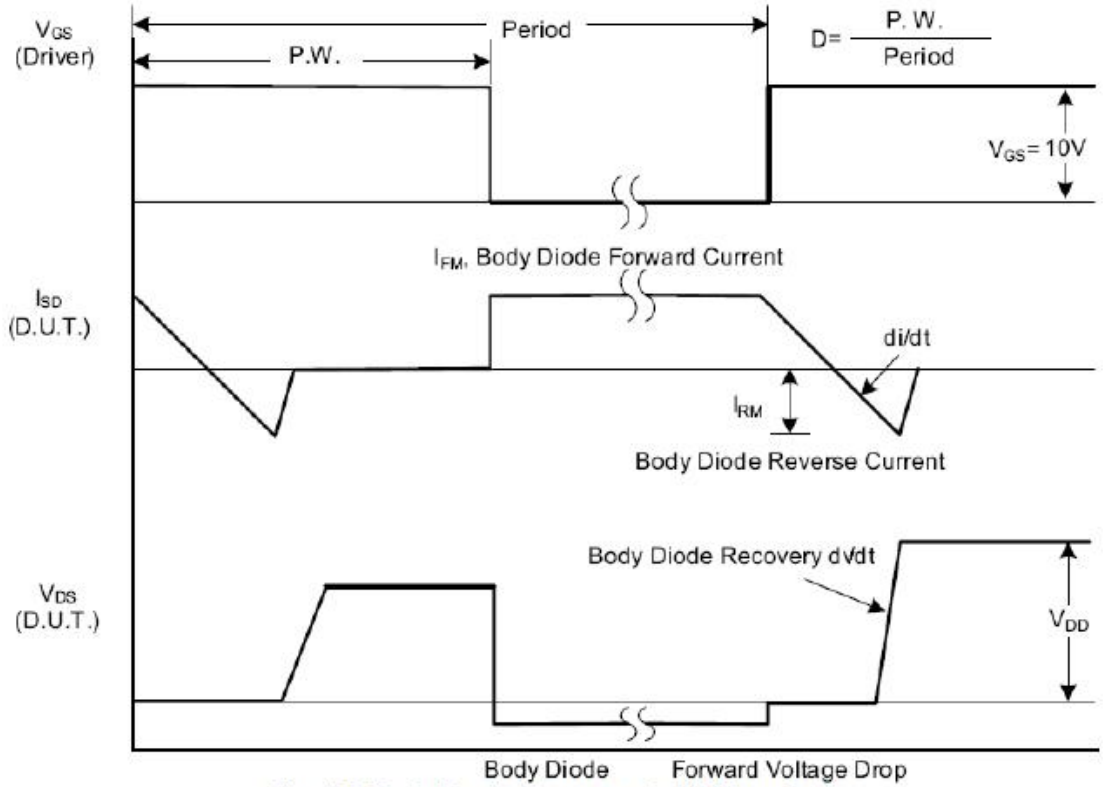


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

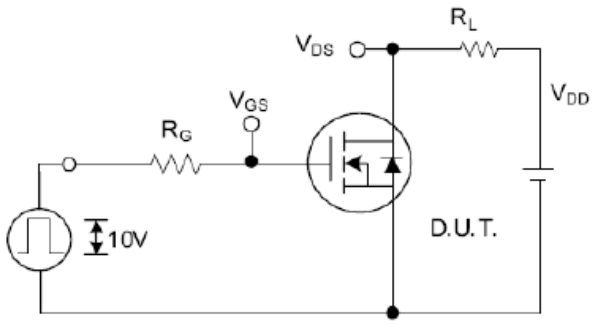


Fig. 2.1 Switching Test Circuit

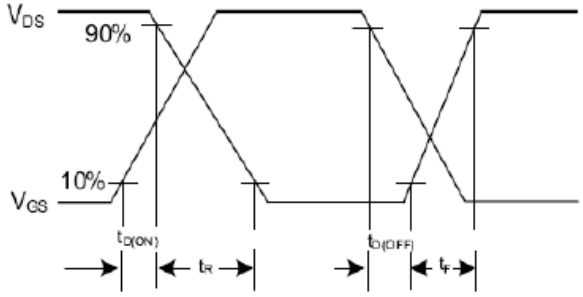


Fig. 2.2 Switching Waveforms

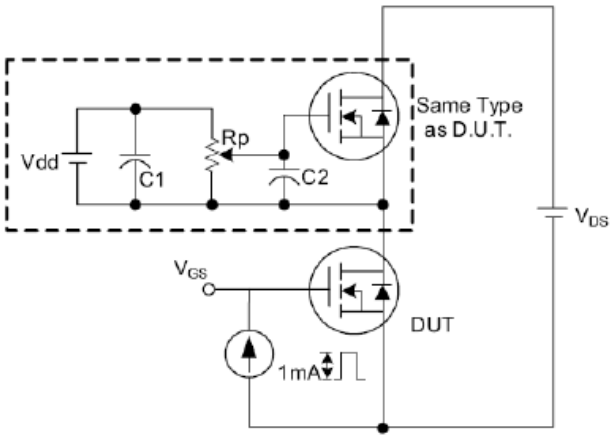


Fig. 3 . 1 Gate Charge Test Circuit

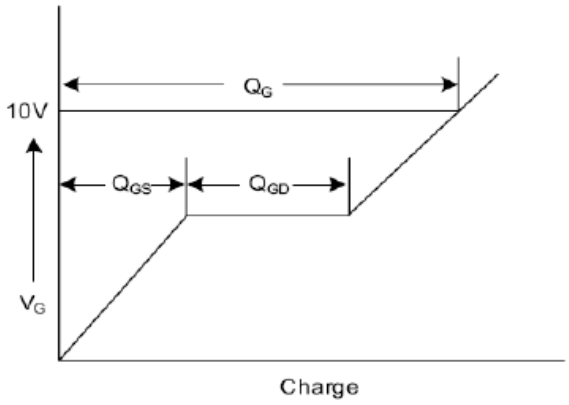


Fig. 3 . 2 Gate Charge Waveform

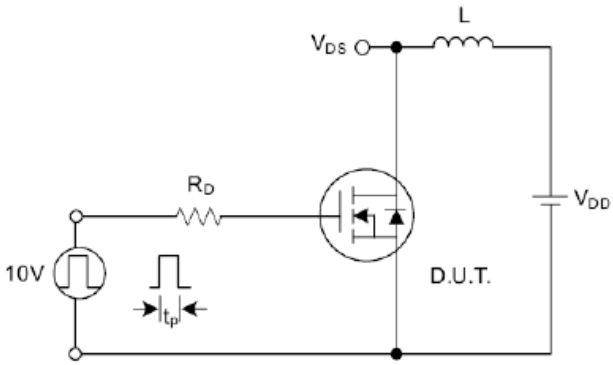


Fig. 4.1 Unclamped Inductive Switching Test Circuit

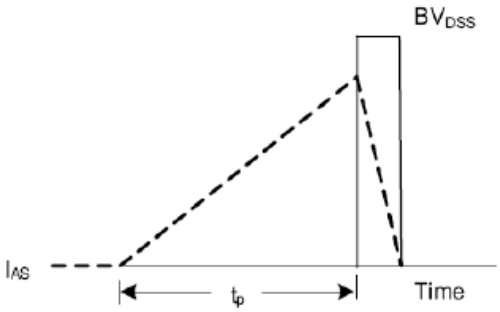


Fig. 4.2 Unclamped Inductive Switching Waveforms